EAST Search

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	6037	(writ$3 program$4) near5 transistor$1 same (read$3 near5 transistor$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/23 08:23
L2	1982	((junction adj field adj effect adj transistor$1) JFET$1) same ((metal adj oxide adj semiconductor adj field adj effect adj transistor$1) MOSFET$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/23 08:22
L12	410	(1 2) same vertical$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/23 08:29
L13	46	12 and (gain adj cell$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/23 08:30

Interference Search

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	292	(((writ$3 program$4) with transistor$1) same (read$3 near5 transistor$1)).clm.	US-PGPUB	OR	OFF	2005/12/23 08:24
L9	4	(8 same (gain adj cell$1)).clm.	US-PGPUB	OR	OFF	2005/12/23 08:25

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Day : Friday
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Time: 08:33:17

Inventor Name Search Result

Your Search was:

Last Name = NOBLE
First Name = WEND

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09052403	6271555	150	03/31/1998	BORDERLESS WORDLINE FOR DRAM CELL	NOBLE JR., WENDELL P.
09076766	6128216	150	05/13/1998	HIGH DENSITY PLANAR SRAM CELL WITH MERGED TRANSISTORS	NOBLE JR., WENDELL P.
09398659	6121128	150	09/17/1999	METHOD FOR MAKING BORDERLESS WORDLINE FOR DRAM CELL	NOBLE JR., WENDELL P.
09052538	6175128	150	03/31/1998	PROCESS FOR BUILDING BODERLESS BITLINE, WORDLINE AND DRAM STRUCTURE AND RESULTING STRUCTURE	NOBLE, JR, WENDELL P.
08365617	6252267	150	12/28/1994	FIVE SQUARE FOLDED-BITLINE DRAM CELL	NOBLE, JR., WENDELL P.
08845609	5892707	150	04/25/1997	MEMORY ARRAY HAVING A DIGIT LINE BURIED IN AN ISOLATION REGION AND METHOD FOR FORMING SAME	NOBLE, WENDELL
09234781	6306703	150	01/20/1999	MEMORY ARRAY HAVING A DIGIT LINE BURIED IN AN ISOLATION REGION AND METHOD FOR FORMING SAME	NOBLE, WENDELL
09900341	6417040	150	07/05/2001	METHOD FOR FORMING MEMORY ARRAY HAVING A DIGIT LINE BURIED IN AN ISOLATION REGION	NOBLE, WENDELL
09517036	6319773	150	03/02/2000	Construction and application for non-volatile, reprogrammable switches	NOBLE, WENDELL P
09131005	6319333	150	08/07/1998	SILICON-ON-INSULATOR ISLANDS	NOBLE, WENDELL P
09144202	6320222	150	09/01/1998	STRUCTURE AND METHOD FOR REDUCING THRESHOLD VOLTAGE VARIATIONS DUE TO DOPANT FLUCTUATIONS	NOBLE, WENDELL P
09494415	6261933	250	01/31/2000	Process for building borderless bitline,	NOBLE, WENDELL P.

				wordline and DRAM structure	
09514493	6294418	150	02/29/2000	Circuits and methods using vertical complementary transistors	NOBLE, WENDELL P.
09520494	6486027	150	03/08/2000	FIELD PROGRAMMABLE LOGIC ARRAYS WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09520649	6191448	150	03/07/2000	Memory cell with vertical transistor and buried word and body lines	NOBLE, WENDELL P.
09527981	6689660	150	03/17/2000	4 F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES	NOBLE, WENDELL P.
09533122	6277701	150	03/23/2000	Circuit and method for a memory cell using reverse base current effect	NOBLE, WENDELL P.
09537602	6194262	150	03/29/2000	Method for coupling to semiconductor device in an integrated circuit having edge-defined, sub-lithographic conductors	NOBLE, WENDELL P.
09551027	6764901	150	04/17/2000	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR	NOBLE, WENDELL P.
09571352	6476434	150	05/16/2000	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES	NOBLE, WENDELL P.
09596266	6399979	150	06/16/2000	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES	NOBLE, WENDELL P.
09605178	6376317	150	06/28/2000	Methods for dual-gated transistors	NOBLE, WENDELL P.
09605911	6414356	150	06/28/2000	CIRCUITS AND METHODS FOR DUAL-GATED TRANSISTORS	NOBLE, WENDELL P.
09609813	6773968	150	07/03/2000	HIGH DENSITY PLANAR SRAM CELL USING BIPOLAR LATCH-UP AND GATED DIODE BREAKDOWN	NOBLE, WENDELL P.
09649983	6340612	150	08/29/2000	METHOD OF FABRICATING BODY CONTACTED AND BACKGATED TRANSISTORS	NOBLE, WENDELL P.
09650600	6498065	150	08/30/2000	MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09651199	6504201	150	08/30/2000	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES	NOBLE, WENDELL P.
09657968	6420748	150	09/08/2000	BORDERLESS BITLINE AND WORDLINE DRAM STRUCTURE	NOBLE, WENDELL P.

09669281	6597037	150	09/26/2000	PROGRAMMABLE MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09694258	6342718	150	10/24/2000	Compact sram cell using tunnel diodes	NOBLE, WENDELL P.
09730102	6633067	150	12/05/2000	COMPACT SOI BODY CONTACT LINK	NOBLE, WENDELL P.
09730245	6610566	150	12/05/2000	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR	NOBLE, WENDELL P.
09731199	6365448	150	12/06/2000	Structure and method for gated lateral bipolar transistors	NOBLE, WENDELL P.
09736547	6509213	150	12/11/2000	Method of forming transistors and connections thereto	NOBLE, WENDELL P.
09742568	6537871	150	12/20/2000	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR	NOBLE, WENDELL P.
09750111	6936886	150	12/29/2000	HIGH DENSITY SRAM CELL WITH LATCHED VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09756089	6515510	150	01/08/2001	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09756099	6486703	150	01/08/2001	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09757683	6489192	150	01/08/2001	BASE CURRENT REVERSAL SRAM MEMORY CELL AND METHOD	NOBLE, WENDELL P.
09779090	6362043	150	02/08/2001	Method for coupling to semiconductor device in an integrated circuit having edge-defined, sub-lithographic conductors	NOBLE, WENDELL P.
09789274	6492233	150	02/20/2001	MEMORY CELL WITH VERTICAL TRANSISTOR AND BURIED WORD AND BODY LINES	NOBLE, WENDELL P.
09819259	6472263	150	03/27/2001	NEGATIVE RESISTANCE MEMORY CELL AND METHOD	NOBLE, WENDELL P.
09848825	6589851	150	05/03/2001	SEMICONDUCTOR PROCESSING METHODS OF FORMING A CONDUCTIVE GRID	NOBLE, WENDELL P.
09848857	6403429	150	05/03/2001	SEMICONDUCTOR PROCESSING METHODS OF FORMING INTEGRATED CIRCUITRY, FORMING CONDUCTIVE LINES, FORMING A CONDUCTIVE GRID, FORMING A	NOBLE, WENDELL P.

				CONDUCTIVE NETWORK, FORMING AN ELECTRICAL INTERCONNECTION TO A NODE LOCATION, FORMING AN ELECTRICAL INTERCONNECTION WITH A TRANSISTOR	
09850764	6580154	150	05/08/2001	METHOD AND APPARATUS ON (110) SURFACES OF SILICON STRUCTURES WITH CONDUCTION IN THE <110> DIRECTION	NOBLE, WENDELL P.
09866938	Not Issued	71	05/29/2001	Ultra high density flash memory	NOBLE, WENDELL P.
09871682	6503790	150	06/04/2001	HIGH DENSITY VERTICAL SRAM CELL USING BIPOLAR LATCHUP INDUCED BY GATED DIODE BREAKDOWN	NOBLE, WENDELL P.
09873650	6777744	150	06/04/2001	CIRCUITS AND METHODS USING VERTICAL, COMPLEMENTARY TRANSISTORS	NOBLE, WENDELL P.
09879592	6756622	150	06/12/2001	VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME	NOBLE, WENDELL P.
09879602	6680864	150	06/12/2001	METHOD FOR READING A VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY	NOBLE, WENDELL P.

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Inventor Name Search Result

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Last Name = NOBL
First Name = WEND

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09896877	Not Issued	71	06/29/2001	Methods of forming electrical connections	NOBLE, WENDELL P.
09911688	6624021	150	07/24/2001	METHOD FOR FORMING GATE SEGMENTS FOR AN INTEGRATED CIRCUIT	NOBLE, WENDELL P.
09924659	6700821	150	08/08/2001	MOSFET TECHNOLOGY FOR PROGRAMMABLE ADDRESS DECODE AND CORRECTION	NOBLE, WENDELL P.
09924738	6477080	150	08/08/2001	CIRCUITS AND METHODS FOR A STATIC RANDOM ACCESS MEMORY USING VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09924850	6449186	150	08/08/2001	CIRCUITS AND METHODS FOR A STATIC RANDOM ACCESS MEMORY USING VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09930521	6946389	150	08/15/2001	BURIED CONDUCTORS	NOBLE, WENDELL P.
09934461	6461926	150	08/21/2001	CIRCUIT AND METHOD FOR A MEMORY CELL USING REVERSE BASE CURRENT EFFECT	NOBLE, WENDELL P.
09964172	6573169	150	09/26/2001	HIGHLY CONDUCTIVE COMPOSITE POLYSILICON GATE FOR CMOS INTEGRATED CIRCUITS	NOBLE, WENDELL P.
09968643	6498739	150	10/01/2001	APPLICATIONS FOR NON-VOLATILE MEMORY CELLS	NOBLE, WENDELL P.
10047477	6638807	150	10/23/2001	TECHNIQUE FOR GATED LATERAL BIPOLAR TRANSISTORS	NOBLE, WENDELL P.
10057225	6964903	150	01/25/2002	METHOD OF FABRICATING A TRANSISTOR ON A SUBSTRATE TO OPERATE AS A FULLY DEPLETED STRUCTURE	NOBLE, WENDELL P.
10087366	6552435	150	03/01/2002	INTEGRATED CIRCUIT WITH CONDUCTIVE LINES DISPOSED WITHIN ISOLATION REGIONS	NOBLE, WENDELL P.

10140296	6800927	150	05/06/2002	MULTIPLE OXIDE THICKNESSES FOR MERGED MEMORY AND LOGIC APPLICATIONS	NOBLE, WENDELL P.
10140297	6887749	150	05/06/2002	MULTIPLE OXIDE THICKNESSES FOR MERGED MEMORY AND LOGIC APPLICATIONS	NOBLE, WENDELL P.
10152842	6624033	150	05/23/2002	TRENCH DRAM CELL WITH VERTICAL DEVICE AND BURIED WORD LINES	NOBLE, WENDELL P.
10162942	6818937	150	06/04/2002	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES	NOBLE, WENDELL P.
10191167	Not Issued	93	07/09/2002	DRAM TECHNOLOGY COMPATIBLE PROCESSOR/MEMORY CHIPS	NOBLE, WENDELL P.
10191329	6741519	150	07/09/2002	DRAM TECHNOLOGY COMPATIBLE PROCESSOR/MEMORY CHIPS	NOBLE, WENDELL P.
10191330	6924194	150	07/09/2002	DRAM TECHNOLOGY COMPATIBLE PROCESSOR/MEMORY CHIPS	NOBLE, WENDELL P.
10191332	6809985	150	07/09/2002	DRAM TECHNOLOGY COMPATIBLE PROCESSOR/MEMORY CHIPS	NOBLE, WENDELL P.
10222997	Not Issued	61	08/19/2002	METHOD OF FORMING VERTICAL SUB-MICRON CMOS TRANSISTORS ON (110), (111), (311), (511), AND HIGHER ORDER SURFACES OF BULK, SOI AND THIN FILM STRUCTURES	NOBLE, WENDELL P.
10227500	Not Issued	71	08/22/2002	Semiconductor processing methods of forming conductive lines	NOBLE, WENDELL P.
10228732	6696330	150	08/27/2002	METHODS, STRUCTURES, AND CIRCUITS FOR TRANSISTORS WITH GATE-TO-BODY CAPACITIVE COUPLING	NOBLE, WENDELL P.
10230244	6812516	150	08/28/2002	FIELD PROGRAMMABLE LOGIC ARRAYS WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
10284984	6699742	150	10/30/2002	BASE CURRENT REVERSAL SRAM MEMORY CELL AND METHOD	NOBLE, WENDELL P.
10302044	Not Issued	93	11/21/2002	A METHOD OF FORMING AT LEAST ONE INTERCONNECTION TO A SOURCE/DRAIN REGION IN SILICON-ON-INSULATOR INTEGRATED CIRCUITRY	NOBLE, WENDELL P.
10304359	6861311	150	11/25/2002	SEMICONDUCTOR PROCESSING METHODS OF FORMING	NOBLE, WENDELL P.

				INTEGRATED CIRCUITRY, FORMING CONDUCTIVE LINES, FORMING A CONDUCTIVE GRID, FORMING A CONDUCTIVE NETWORK, FORMING AN ELECTRICAL INTERCONNECTION TO A NODE LOCATION, FORMING AN ELECTRICAL INTERCONNECTION WITH A TRANSISTOR SO	
10304659	6884687	150	11/25/2002	SEMICONDUCTOR PROCESSING METHODS OF FORMING INTEGRATED CIRCUITRY, FORMING CONDUCTIVE LINES, FORMING A CONDUCTIVE GRID, FORMING A CONDUCTIVE NETWORK, FORMING AN ELECTRICAL INTERCONNECTION TO A NODE LOCATION, FORMING AN ELECTRICAL INTERCONNECTION WITH A TRANSISTOR SO	NOBLE, WENDELL P.
10305549	6747305	150	11/26/2002	MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
10361986	6798009	150	02/11/2003	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR	NOBLE, WENDELL P.
10463261	6960821	150	06/17/2003	METHOD AND APPARATUS ON (110) SURFACES OF SILICON STRUCTURES WITH CONDUCTION IN THE <110> DIRECTION	NOBLE, WENDELL P.
10626777	6891213	150	07/23/2003	BASE CURRENT REVERSAL SRAM MEMORY CELL AND METHOD	NOBLE, WENDELL P.
10630427	Not Issued	71	07/29/2003	Semiconductor processing methods of forming integrated circuitry, forming conductive lines, forming a conductive grid, forming a conductive network, forming an electrical interconnection to a node location, forming an electrical interconnection with a transistor source/drain region, and integrated circuitry	NOBLE, WENDELL P.
10640387	6946700	150	08/14/2003	TRENCH DRAM CELL WITH VERTICAL DEVICE AND BURIED WORD LINES	NOBLE, WENDELL P.
10665327	6858504	150	09/19/2003	METHOD FOR FORMING GATE SEGMENTS FOR AN INTEGRATED	NOBLE, WENDELL P.

				CIRCUIT	
10705185	Not Issued	120	11/11/2003	Buried conductors	NOBLE, WENDELL P.
10738449	Not Issued	71	12/16/2003	VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME	NOBLE, WENDELL P.
10763136	6909635	150	01/22/2004	PROGRAMMABLE MEMORY CELL USING CHARGE TRAPPING IN A GATE OXIDE	NOBLE, WENDELL P.
10795516	Not Issued	71	03/09/2004	High density SRAM cell with latched vertical transistors	NOBLE, WENDELL P.
10879378	Not Issued	93	06/29/2004	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR	NOBLE, WENDELL P.
10929281	Not Issued	41	08/30/2004	Multiple oxide thicknesses for merged memory and logic applications	NOBLE, WENDELL P.
10930213	Not Issued	94	08/31/2004	METHOD AND APPARATUS ON (110) SURFACES OF SILICON STRUCTURES WITH CONDUCTION IN THE <110> DIRECTION	NOBLE, WENDELL P.
10962657	Not Issued	30	10/13/2004	Trench DRAM cell with vertical device and buried word lines	NOBLE, WENDELL P.
11214557	Not Issued	30	08/30/2005	Circuit and method for a folded bit line memory cell with vertical transistor and trench capacitor	NOBLE, WENDELL P.
11234241	Not Issued	18	09/26/2005	High density SRAM cell with latched vertical transistors	NOBLE, WENDELL P.
11235041	Not Issued	20	09/26/2005	Buried conductors	NOBLE, WENDELL P.
06200851	4380057	150	10/27/1980	ELECTRICALLY ALTERABLE DOUBLE DENSE MEMORY	NOBLE, WENDELL P.
06627250	4609429	150	07/02/1984	PROCESS FOR MAKING A SMALL DYNAMIC MEMORY CELL STRUCTURE	NOBLE, WENDELL P.
06793509	4675982	150	10/31/1985	METHOD OF MAKING SELF-ALIGNED RECESSED OXIDE ISOLATION REGIONS	NOBLE, WENDELL P.
07135953	Not Issued	166	12/21/1987	METHOD FOR PROVIDING BRIDGE CONTACT BETWEEN SILICON REGIONS SEPARATED BY A THIN DIELECTRIC	NOBLE, WENDELL P.

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
07240421	4873205	150	09/01/1988	METHOD FOR PROVIDING SILICIDE BRIDGE CONTACT BETWEEN SILICON REGIONS SEPERATED BY A THIN DIELECTRIC	NOBLE, WENDELL P.
08056090	5422294	150	05/03/1993	METHOD OF MAKING A TRENCH CAPACITOR FIELD SHIELD WITH SIDEWALL CONTACT	NOBLE, WENDELL P.
08355942	5512767	150	12/13/1994	TRENCH CAPACITOR FIELD SHIELD WITH SIDEWALL CONTACT	NOBLE, WENDELL P.
08365729	5539229	150	12/28/1994	MOSFET WITH RAISED STI ISOLATION SELF-ALIGNED TO THE GATE STACK	NOBLE, WENDELL P.
08366517	5650654	250	12/30/1994	MOSFET DEVICE HAVING CONTROLLED PARASITIC ISOLATION THRESHOLD VOLTAGE	NOBLE, WENDELL P.
08481675	5598367	150	06/07/1995	TRENCH EPROM	NOBLE, WENDELL P.
08544498	6090660	150	10/18/1995	METHOD OF FABRICATING A GATE CONNECTOR	NOBLE, WENDELL P.
08580816	5908310	150	12/27/1995	METHOD TO FORM A BURIED IMPLANTED PLATE FOR DRAM TRENCH STORAGE CAPACITORS	NOBLE, WENDELL P.
08598444	5930619	250	02/08/1996	METHOD OF MAKING TRENCH EPROM SIMULTANEOUSLY WITH FORMING A DRAM CELL	NOBLE, WENDELL P.
08679799	6180972	150	07/15/1996	BURIED, IMPLANTED PLATE FOR DRAM TRENCH STORAGE CAPACITORS	NOBLE, WENDELL P.
08745708	6211039	150	11/12/1996	SILICON-ON-INSULATOR ISLANDS AND METHOD FOR THEIR FORMATION	NOBLE, WENDELL P.
08760090	5932908	150	12/11/1996	TRENCH EPROM	NOBLE, WENDELL P.

08771570	Not Issued	161	12/20/1996	POLY-ALUMINUM EXCHANGE FOR ALUMINUM FILL OF HIGH ASPECT RATIO SHAPES	NOBLE, WENDELL P.
08772708	6022781	150	12/23/1996	A METHOD FOR FABRICATING A MOSFET WITH RAISED STI ISOLATION SELF- ALIGNED TO THE GATE STACK	NOBLE, WENDELL P.
08841967	5873053	150	04/08/1997	ON-CHIP THERMOMETRY FOR CONTROL OF CHIP OPERATING TEMPERATURE	NOBLE, WENDELL P.
08842950	6190960	150	04/25/1997	METHOD FOR COUPLING TO SEMICONDUCTOR DEVICE IN AN INTEGRATED CIRCUIT HAVING EDGE-DEFINED SUB-LITHOGRAPHIC CONDUCTORS	NOBLE, WENDELL P.
08842971	5976930	150	04/25/1997	METHOD FOR FORMING GATE SEGMENTS FOR AN INTEGRATED CIRCUIT	NOBLE, WENDELL P.
08846110	6004835	150	04/25/1997	METHOD OF FORMING INTEGRATED CIRCUITRY, CONDUCTIVE LINES, A CONDUCTIVE GRID, A CONDUCTIVE NETWORK, AN ELECTRICAL INTERCONNECTION TO ANODE LOCATION AND AN ELECTRICAL INTERCONNECTION WITH A TRANSISTOR SOURCE/ DRAIN REGION	NOBLE, WENDELL P.
08870336	5953607	150	06/06/1997	NOVEL BURIED STRAP FOR TRENCH STORAGE CAPACITORS IN DRAM TRENCH CELLS	NOBLE, WENDELL P.
08889396	5909618	150	07/08/1997	METHOD OF MAKING MEMORY CELL WITH VERTICAL TRANSISTOR AND BURIED WORD AND BODY LINES	NOBLE, WENDELL P.
08889462	6150687	150	07/08/1997	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES	NOBLE, WENDELL P.
08889463	6072209	150	07/08/1997	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES	NOBLE, WENDELL P.
08889553	5936274	150	07/08/1997	YIGH DENSITY FLASH MEMORY	NOBLE, WENDELL P.
08889554	5973356	150	07/08/1997	ÙLTRA HIGH DENSITY FLASH MEMORY	NOBLE, WENDELL P.
08915197	5973352	150	08/20/1997	ULTRA HIGH DENSITY FLASH	NOBLE, WENDELL P.

				MEMORY HAVING VERTICALLY STACKED DEVICES	
08939732	5907170	150	10/06/1997	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR	NOBLE, WENDELL P.
08939742	6066869	150	10/06/1997	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR	NOBLE, WENDELL P.
08944312	5914511	150	10/06/1997	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY USING TRENCH PLATE CAPACITOR CELLS WITH BODY BIAS CONTACTS	NOBLE, WENDELL P.
08944890	6528837	150	10/06/1997	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR	NOBLE, WENDELL P.
08965143	5987196	150	11/06/1997	SEMICONDUCTOR STRUCTURE HAVING AN OPTICAL SIGNAL PATH IN A SUBSTRATE AND METHOD FOR FORMING THE SAME	NOBLE, WENDELL P.
09028727	6304483	150	02/24/1998	CIRCUITS AND METHODS FOR A STATIC RANDOM ACCESS MEMORY USING VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09028805	6242775	150	02/24/1998	CIRCUITS AND METHODS USING VERTICAL COMPLEMENTARY TRANSISTORS	NOBLE, WENDELL P.
09028807	6246083	150	02/27/1998	VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY	NOBLE, WENDELL P.
09031620	6104061	150	02/27/1998	MEMORY CELL WITH VERTICAL TRANSISTOR AND BURIED WORD AND BODY LINES	NOBLE, WENDELL P.
09031621	5991225	150	02/27/1998	PROGRAMMABLE MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09031637	6492694	150	02/27/1998	HIGHLY CONDUCTIVE COMPOSITE POLYSILICON GATE FOR CMOS INTEGRATED CIRCUITS	NOBLE, WENDELL P.
09031960	6448615	150	02/26/1998	METHODS, STRUCTURES, AND CIRCUITS FOR TRANSISTORS WITH GATE-TO-BODY CAPACITIVE COUPLING	NOBLE, WENDELL P.

09032617	6124729	150	02/27/1998	FIELD PROGRAMMABLE LOGIC ARRAYS WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09035304	6238976	150	02/27/1998	A METHOD FOR FORMING HIGH DENSITY FLASH MENORY	NOBLE, WENDELL P.
09042795	6046477	150	03/17/1998	A DENSE SOI PROGRAMMABLE LOGIC ARRAY STRUCTURE	NOBLE, WENDELL P.
09050266	6075272	150	03/30/1998	STRUCTURE FOR GATED LATERAL BIPOLAR TRANSISTORS	NOBLE, WENDELL P.
09050275	6229342	150	03/30/1998	CIRCUITS AND METHODS FOR BODY CONTACTED AND BACKGATED TRANSISTORS	NOBLE, WENDELL P.
09050281	6097065	150	03/30/1998	CIRCUITS AND METHODS FOR DUAL-GATED TRANSISTORS	NOBLE, WENDELL P.
09050443	6049496	150	03/30/1998	CIRCUIT AND METHOD FOR LOW VOLTAGE, CURRENT SENSE AMPLIFIER	NOBLE, WENDELL P.
09050579	6107663	150	03/30/1998	CIRCUIT AND METHOD FOR GATE-BODY STRUCTURES IN CMOS TECHNOLOGY	NOBLE, WENDELL P.
09050615	6104066	150	03/30/1998	CIRCUIT AND METHOD FOR LOW VOLTAGE,VOLTAGE SENSE AMPLIFIER	NOBLE, WENDELL P.
09050728	6307235	150	03/30/1998	ANOTHER TECHNIQUE FOR GATED LATERAL BIPOLAR TRANSISTORS	NOBLE, WENDELL P.
09055347	6215145	150	04/06/1998	DENSE SOI FLASH MEMORY ARRAY STRUCTURE	NOBLE, WENDELL P.
09069326	6696746	150	04/29/1998	BURIED CONDUCTORS	NOBLE, WENDELL P.
09076487	6545297	150	05/13/1998	HIGH DENSITY VERTICAL SRAM CELL USING BIPOLAR LATCHUP INDUCED BY GATED DIODE BREAKDOWN	NOBLE, WENDELL P.

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
09076728	6225165	150	05/13/1998	HIGH DENSITY SRAM CELL WITH LATCHED VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09076745	6104045	150	05/13/1998	HIGH DENSITY PLANAR SRAM CELL USING BIPOLAR LATCH-UP AND GATED DIODE BREAKDOWN	NOBLE, WENDELL P.
09128848	6134175	150	08/04/1998	MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09129047	6208164	150	08/04/1998	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS	NOBLE, WENDELL P.
09130989	6204145	150	08/07/1998	SILICON-ON-INSULATOR ISLANDS AND METHOD FOR THEIR FORMATION	NOBLE, WENDELL P.
09137328	6143636	150	08/20/1998	HIGH DENSITY FLASH MEMORY	NOBLE, WENDELL P.
09138794	6165836	150	08/24/1998	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR	NOBLE, WENDELL P.
09138796	6156607	150	08/24/1998	METHOD FOR A FOLDED BIT LINE MEMORY USING TRENCH PLATE CAPACITOR CELLS WITH BODY BIAS CONTACTS	NOBLE, WENDELL P.
09139164	6350635	150	08/24/1998	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES	NOBLE, WENDELL P.
09143606	6156604	150	08/31/1998	METHOD FOR MAKING AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR	NOBLE, WENDELL P.
09144811	6165828	150	09/01/1998	STRUCTURE AND METHOD FOR GATED LATERAL BIPOLAR	NOBLE, WENDELL P.

				TRANSISTORS	
09145582	6072223	150	09/02/1998	CIRCUIT AND METHOD FOR A MEMORY CELL USING REVERSE BASE CURRENT EFFECT	NOBLE, WENDELL P.
09146301	6156589	150	09/03/1998	COMPACT SOI BODY CONTACT LINK	NOBLE, WENDELL P.
09195163	6316305	150	11/18/1998	COMPACT SRAM CELL USING TUNNEL DIODES	NOBLE, WENDELL P.
09204072	5977579	150	12/03/1998	TRENCH DRAM CELL WITH VERTICAL DEVICE AND BURIED WORD LINES	NOBLE, WENDELL P.
09249288	6373138	150	02/10/1999	AN INTEGRATED CIRCUIT WITH CONDUCTIVE LINES DISPOSED WITHIN ISOLATION REGIONS	NOBLE, WENDELL P.
09259493	6380581	150	02/26/1999	DRAM TECHNOLOGY COMPATIBLE NON VOLATILE MEMORY CELLS	NOBLE, WENDELL P.
09261479	6256225	150	02/26/1999	CONSTRUCTION AND APPLICATION FOR NON-VOLATILE, REPROGRAMMABLE SWITCHES	NOBLE, WENDELL P.
09261597	6297989	150	02/26/1999	APPLICATIONS FOR NON-VOLATILE MEMORY CELLS	NOBLE, WENDELL P.
09261598	6452856	150	02/26/1999	DRAM TECHNOLOGY COMPATIBLE PROCESSOR/MEMORY CHIPS	NOBLE, WENDELL P.
09268823	6313490	150	03/16/1999	BASE CURRENT REVERSAL SRAM MEMORY CELL AND METHOD	NOBLE, WENDELL P.
09281197	6208555	150	03/30/1999	NEGATIVE RESISTANCE MEMORY CELL AND METHOD	NOBLE, WENDELL P.
09310037	6348366	150	05/11/1999	METHOD OF FORMING CONDUCTIVE LINES	NOBLE, WENDELL P.
09310043	6300204	150	05/11/1999	SEMICONDUCTOR PROCESSING METHODS OF FORMING INTEGRATED CIRCUITRY, FORMING CONDUCTIVE LINES, FORMING A CONDUCTIVE GRID, FORMING A CONDUCTIVE NETWORK, FORMING AN ELECTRICAL INTERCONNECTION TO A NODE LOCATION, FORMING AN ELECTRICAL INTERCONNECTION WITH A TRANSISTOR SOUR	NOBLE, WENDELL P.
09310044	6344399	150	05/11/1999	METHOD OF FORMING CONDUCTIVE LINES AND METHOD OF FORMING A CONDUCTIVE GRID	NOBLE, WENDELL P.
09313049	6153468	150	05/17/1999	A METHOD OF FORMING A LOGIC ARRAY FOR A DECODER	NOBLE, WENDELL P.

09323493	6060754	150	06/01/1999	CIRCUIT AND METHOD FOR GATE-BODY STRUCTURES IN CMOS TECHNOLOGY	NOBLE, WENDELL P.
09371750	6091654	150	08/10/1999	CIRCUIT AND METHOD FOR LOW VOLTAGE, CURRENT SENSE AMPLIFIER	NOBLE, WENDELL P.
09373357	6190950	150	08/12/1999	DENSE SOI PROGRAMMABLE LOGIC ARRAY STRUCTURE	NOBLE, WENDELL P.
09383804	6521958	150	08/26/1999	MOSFET TECHNOLOGY FOR PROGRAMMABLE ADDRESS DECODE AND CORRECTION	NOBLE, WENDELL P.
09385380	6141238	150	08/30/1999	DYNAMIC RANDOM ACCESS MEMORY (DRAM) CELLS WITH REPRESSED FERROELECTRIC MEMORY METHODS OF READING SAME, AND APPARATUSES INCLUDING SAME	NOBLE, WENDELL P.
09386181	6245615	150	08/31/1999	METHOD AND APPARATUS ON (110) SURFACES OF SILICON STRUCTURES WITH CONDUCTION IN THE <110> DIRECTION	NOBLE, WENDELL P.
09386185	6383871	150	08/31/1999	METHOD OF FORMING MULTIPLE OXIDE THICKNESSES FOR MERGED MEMORY AND LOGIC APPLICATIONS	NOBLE, WENDELL P.
09386313	6483171	150	08/13/1999	VERTICAL SUB-MICRON CMOS TRANSISTORS ON (110), (111), (311), (511), AND HIGHER ORDER SURFACES OF BULK, SOI AND THIN FILM STRUCTURES AND METHOD OF FORMING SAME	NOBLE, WENDELL P.
09386315	6436748	150	08/31/1999	METHOD FOR FABRICATING CMOS TRANSISTORS HAVING MATCHING CHARACTERISTICS AND APPARATUS FORMED THEREBY	NOBLE, WENDELL P.
09405091	6395597	150	09/27/1999	TRENCH DRAM CELL WITH VERTICAL DEVICE AND BURIED WORD LINES	NOBLE, WENDELL P.
09414426	6255171	150	10/07/1999	METHOD OF MAKING DENSE SOI FLASH MEMORY ARRAY STRUCTURE	NOBLE, WENDELL P.
09426451	6211015	150	10/25/1999	ULTRA HIGH DENSITY FLASH MEMORY HAVING VERTICALLY STACKED DEVICES	NOBLE, WENDELL P.
09430442	6266268	150	10/29/1999	METHOD FOR FORMING GATE SEGMENTS FOR AN INTEGRATED	NOBLE, WENDELL P.

				CIRCUIT	
09451982	6235569	150	11/30/1999	CIRCUIT AND METHOD FOR LOW VOLTAGE, VOLTAGE SENSE AMPLIFIER	NOBLE, WENDELL P.
09461009	6337805	150	12/15/1999	DISCRETE DEVICES INCLUDING EAPROM TRANSISTOR AND NVRAM MEMORY CELL WITH EDGE DEFINED FERROELECTRIC CAPACITANCE, METHODS FOR OPERATING SAME, AND APPARATUS INCLUDING SAME	NOBLE, WENDELL P.
05973219	4222816	150	12/26/1978	METHOD FOR REDUCING PARASITIC CAPACITANCE IN INTEGRATED CIRCUTT STRUCTURES	NOBLE, WENDELL PHILLIPS
08743955	5726095	250	10/28/1996	METHOD OF MAKING MOSFET DEVICE HAVING CONTROLLED PARASITIC ISOLATION THRESHOLD VOLTAGE	NOBLE, WENDELL PHILLIPS

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